Express Mail Number: ELO52826940US Docket No. B-3604 616923-4

Date: February 8, 1999

Commissioner of Patents and Trademarks
Box Patent Application
Washington, D.C. 20231

Sir:

NEW APPLICATION TRANSMITTAL

Transmitted herewith for filing is the patent application of

Inventor(s): Pascal OUDET

NOTE: Patent must be applied for in the name of all of the actual inventor or inventors.

For: "ADDRESS REMAPPING FOR A BUS"

Enclosed are:

The Papers Required For Filing Date Under 37 CFR 1.53(b):

13 Pages of specification 1 Page of abstract 2 Pages of claims

2 Sheets of drawings [X] formal [ ] informal
(Figs. 1-5)

[X] In addition to the above papers there is also attached
2 Pages of an amendment dated February 8, 1999 .

postcard
Check for filing fee in the amount of $838.00
Declaration/Power of Attorney (3 pages)
Claim to Priority (1 page) with certified copy of EP Appln. No. 98400760.9
IDS Form 1449 (modified)- 1 page)) with copies of three cited documents and cover letter (1 page)

CERTIFICATION UNDER 37 CFR 1.10

I hereby certify that this paper and the documents referred to as enclosed therein are being deposited with the United States Postal Service in an Express Mail envelope with sufficient postage for Express Mailing on this date February 8, 1999 in an envelope as "Express Mail Post Office to Addressee" Mailing Label Number **ELO52826940US** addressed to the:

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NOTE: Each paper or fee referred to as enclosed herein has the number of the "Express Mail" mailing label placed thereon prior to mailing. 37 CFR 1.10(b).

2. **Declaration or oath**

[X] Enclosed

[X] original [ ] facsimile

executed by:

[X] inventor(s)

[ ] legal representative of inventor(s) 37 CFR 1.42 or 1.43

[ ] joint inventor or person showing a proprietary interest on behalf of inventor who refused to sign or cannot be reached. 37 CFR 1.47.

[ ] petition and statement required by 37 CFR 1.47 also attached. See item 7 below for fee.

[ ] Not Enclosed

[ ] Application is made by a person authorized under 37 CFR 1.41(c) on behalf of all of the above named inventor(s). The declaration or oath, along with the surcharge required by 37 CFR 1.16(e) can be filed subsequently.

[ ] Showing that the filing is authorized. (Not required unless called into question. 37 CFR 1.41(d)).

NOTE: Where the filing is a completion in the U.S. of an international application under 35 U.S.C. 371(c)(4) then the declaration must be filed.

3. **Assignment**

[ ] An assignment of the invention to _____

_____

4. **Certified Copy**

[X] A certified copy of EP application(s) No. 98400760.9

_____

from which priority is claimed.

NOTE: Must be referred to in oath or declaration. 37 CFR 1.55 and 163.

5. **Fee Calculation**

CLAIMS AS FILED					
Number Filed		**Number Extra**		**Rate**	**Basic Fee $ 760.00**
Total Claims 15 -20=		0	x	$ 18.00	0
Independent Claims 4 -3=		1	x	$ 78.00	78.00
Multiple Dependent Claim(s), If Any		0	x	$260.00	0

[ ] Amendment cancelling extra claims enclosed

[x] Amendment deleting multiple dependencies enclosed

[ ] Fee for extra claims is not being paid at this time

NOTE: If the fee for extra claims are not paid on filing they must be paid or the claims cancelled by amendment, prior to the expiration of the time period set for response by the Patent and Trademark Office in any notice of fee deficiency, 37 CFR 1.16(d).

Filing Fee Calculation $ 838.00

6. **Small Entity Statement**

[ ] Verified statement that this is a filing by a small entity under 37 CFR 1.9 and 1.27.

Filing Fee Calculation (50% of above) $_____

NOTE: If a verified statement is filed within 2 months of the date of payment of first fee then the excess fee paid will be refunded on request. Notice of January 20, 1983. 1027 TMOG 114.

7. **Fee Payment Being Made At This Time**

[ ] Not Enclosed

[ ] No filing fee is submitted. This and the surcharge required by 37 CFR 1.16(e) can be paid subsequently.

NOTE: Where the filing is a completion in the U.S. of an international application the fee must be paid.

[X] Enclosed

[X] filing fee	$ 838.00
[ ] recording assignment ($40.00; 37 CFR 1.21(h)(i))	$_____
[ ] petition fee for filing by other than all the inventors or person on behalf of the inventor where inventor refused to sign or cannot be reached. 37 CFR 1.47 and 1.17 (h)	$_____
Total fees enclosed	$ 838.00

8. **Method of Payment of Fees**

[X] check in the amount of $ 838.00

[ ] charge account No. 12-0415 in the amount of $_____
A duplicate of this transmittal is attached.

NOTE: Fees should be itemized is such a manner that it is clear for which purpose the fees are paid. 37 CFR 1.22(b).

9. **Authorization to Charge Additional fees**

[X] The Commissioner is hereby authorized to charge the following additional fees which may be required to Account No. 12-0415:

[X] 37 CFR 1.16 (filing fees and presentation of extra claims)

[X] 37 CFR 1.17 (application processing fees)

[ ] 37 CFR 1.18 (issue fee at or before Mailing of Notice of Allowance, pursuant to 37 CFR 1.311(b))

NOTE: 37 CFR 1.28(b) requires "Notification of any change in loss of entitlement to small entity status must be filed in the application ...prior to paying... issue fee".

10. **Instructions As To Overpayment**

[X] Credit Account No. 12-0415 [ ] refund

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EXPRESS MAIL EL052826940US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Pascal OUDET | Re: Preliminary Amendment

Serial No.: | Our Ref: B-3604 616923-4

Filed: Concurrently herewith | Date: February 8, 1999

For: "ADDRESS REMAPPING FOR A BUS"

BOX PATENT APPLICATION
Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Prior to examination of the above-identified application, it is respectfully requested that the following amendments be made to the claims and abstract:

IN THE CLAIMS

Claim 1,	line 1	Please delete "(1)".
	line 2	Please delete "(3, 4)".
	line 3	Please delete "(5-9)".
Claim 3,	line 1	Please delete "or 2".
Claim 4,	line 2	Please delete "(21-24)".
	line 3	Please delete "(30)".
	line 5	Please delete "(32, 26, 24)".
Claim 5,	line 2	Please delete "(30)".
Claim 6,	line 1	Please delete "or 5".
	last line	Please delete "(34)".
Claim 7,	line 1	Please delete "5 or 6",".
	line 3	Please delete "(23, 24)".

Claim 8, last line Please delete "(21, 22)".

Please add the following new claims:

--13. A computer system including a bus, having at least an address remapper defining two sections in the bus, each section comprising at least one station having a physical address, wherein a station on one section of the bus is assigned a dummy address for being addressed by a station on the other section, the address remapper remapping a dummy address from the other section into a physical address to the one section.

14. A computer system according to claim 13, wherein the format of a physical address comprises a fixed part and a setable part, and wherein the dummy address is obtained by changing at least one bit of the fixed part of the physical address.

15. A computer system according to claim 13, wherein the dummy addresses for stations out of a given section are different from the physical addresses for stations in said given section.--

IN THE ABSTRACT

Line 1	Please delete "(1)".
Line 2	Please delete "(3, 4)".
Last line	Please delete "(Fig. 1)".

REMARKS

Amendment of the subject application is respectfully requested.

Respectfully submitted,

Richard J. Paciulan
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Address remapping for a bus

Field of the Invention

The present invention relates to a bus, having at least an address remapper defining two sections in the bus. It also relates to an address remapper for such a bus, and to a process for connecting two sections of a bus. It applies particularly to two-wire serial buses.

Background of the Invention

A bus is comprised of an assembly of wires intended to transfer information between stations connected on the bus.

US-A-4689740 discloses a two wire serial bus system, comprising a clock wire and a data wire, for interconnecting a number of stations. The system disclosed in this specification is promoted by Philips Semiconductors under the name I2C bus. The number of stations connected to this bus system is limited by the size of the address of the stations. A similar two wire serial bus system is also sold under the reference SMBus (system management bus) by Intel. In the rest of the present specification, the terms I2C will be used as a generic term for such two wire serial bus systems.

This bus system comprises two wires, that is a data wire and a clock wire. The data wire is normally at a high level and may be brought to a low level by any station connected to the bus. START and STOP conditions are defined as a transition of the value of the data wire while the clock wire is at a high level; a START condition is followed by an address. For more details on the structure and operation of the I2C bus system, reference should be made to the document 'The I2C bus and how to use it (including specifications)' Philips Semiconductors, April 1995.

One problem in I2C buses is the use of similar stations. Generally such stations are provided as ICs having an address comprised of a fixed part and of a setable part; the setable part of the address can be set by the user of the IC, at the time the station is used.

Such addresses further limit the number of identical stations used on the same I2C bus. For instance, for an address mapped on 8 bits, with the last bit used for indicating the read-write direction, four bits of the address may be fixed by the founder of the IC, thus leaving only 3 bits of address setable by the user. Under such circumstances, it is not possible to have more than 8 similar stations on the same bus. In existing serial eeproms on the market, the address format is 1010xyzR (binary format), where x, y and z are configurable by the user; a maximum of 8 eeproms is thus allowed on the bus.

Another problem with an I2C bus is that it is impossible on such a bus to have two distinct stations having the same physical address. This prevents using the same chip twice.

Accordingly, the address scheme of I2C is a limitation to the use of similar or identical stations on the bus system. There exists a need for a solution allowing the use of similar or identical stations on an I2C type bus, or on similar types of two wire buses, or more generally on all types of buses.

Summary of the Invention

According to the invention, there is provided a bus, having at least an address remapper defining two sections in the bus, each section comprising at least one station having a physical address, wherein a station on one section of the bus is assigned a dummy address for being addressed by a station on the other section, the address remapper remapping a dummy address from the other section into a physical address to the one section.

In one embodiment, the format of a physical address comprises a fixed part and a setable part, and the dummy address is obtained by changing at least one bit of the fixed part of the physical address.

In this case, the dummy addresses for stations out of a given section are preferably different from the physical addresses for stations in said given section.

According to the invention, there is also provided an address remapper for a bus, comprising
- terminals for connecting two sections of the bus;
- address detecting means for detecting an address received from one section of the bus;
- address remapping means for remapping the address and transmitting the remapped address to the other section of the bus.

Preferably, the bus is a two wire serial bus, and the address detecting means detect a transition of the value on one wire while the other wire is at a given level.

In another embodiment, the bus is a two wire serial bus, and the address remapping means comprise means for bringing one wire to a given level.

The bus may also be a two wire serial bus having one data wire and one clock wire, the terminals for the clock wire of each section being connected. In this case, the address remapping means may comprise switching means for selectively connecting the terminals for the data wire of each section.

Finally, there is provided a process for connecting two sections of a bus, by transmitting data from one section of the bus to the other section of the bus, comprising the steps of
- detecting an address sent from one section of the bus to the other section of the bus;
- remapping the address before transmitting it to the other section of the bus.

Preferably, the step of detecting comprises detecting a START condition preceding an address.

The step of remapping may comprise changing at least one bit of an address, preferably one bit of a fixed part of an address.

Brief Description of the Invention

A bus system embodying the invention will now be described, by way of non-limiting example, with reference to the accompanying drawings, in which

. **Figure 1** is a schematic drawing of a bus system according to the invention;

. **Figure 2** is a schematic diagram of an address remapper according to the invention;

. **Figure 3** shows the timing of signals in a two wire serial bus;

. Figure 4 is a flowchart of the operation of the address remapper of figure 2;

. **Figure 5** is a schematic drawing of an address remapper according to another embodiment of the invention.

Best Mode of Carrying out the Invention

The invention is directed to overcoming the problems of the prior art as regards the addressing of the stations in a bus. It is examplified in the rest of the present description as regards a two wire serial bus system having a data wire and a clock wire. The basic operation of such a bus system is based on the definition of STOP and START conditions, that correspond to a given change on the data line while the clock line is at a high level. The invention is however not limited to such a bus system, but applies to all kind of buses.

The invention suggests using an address remapper for defining different sections in the bus, and remapping the address in each section. Figure 1 is a schematic drawing of a bus system according to the invention, in the simplest configuration where the bus comprises one address remapper 1 defining two sections on the serial bus: the first section 3 is on one side of the address remapper - the left side on figure 1, and the other section 5 is on the other side of the address remapper - the right side on figure 1. On each section 3, 4 of the bus, there may be several stations, and by way of example, the bus system of figure 1 comprises three stations 5, 7 and 9 on the left side and two stations 6 and 8 on the right side. For instance, assuming the address format of each station is

1010xyzR, as in the existing eeproms stations, table I gives a possible set of addresses for the stations:

Table I

station	address
5	1010001
7	1010010
9	1010011
6	1010001
8	1010010

Addresses in table I are the physical addresses of each station, that is the address configured in each station according to the existing I2C specification. In other words, a message sent on the left section of the bus, with an address 1010001 will be considered and processed by station 5, and ignored by stations 7 and 9. As exemplified in this table, station 5 on the left section of the bus and station 6 on the right section of the bus have the same physical address 1010001, while station 7 on the left section of the bus and station 8 on the right section of the bus have the same physical address 1010010. It is clear that such stations cannot possibly be used on the same two wire serial bus according to the prior art.

The operation of the bus of figure 1 is the following. In each section of the bus, the operation is the same one as in the prior art bus. Thus, existing eeproms may also be used for the stations in a bus according to the invention. However, according to the invention, the physical address of the stations of each section is remapped into dummy addresses for the stations of the other sections. Thus, one station on one section of the bus according to the invention sees the stations on the same section with their physical addresses - and thus sees itself with its physical address; however, one station on one section of the bus according to the invention sees the stations on other sections of the bus with dummy addresses that differ from their physical address. The address remapper, when passing a message on the bus from one section to another, will change the dummy address into a physical address.

In the example of figure 1, the following scheme is used for the dummy addresses. Table II gives the addresses of stations on the right section of the bus, as they are sent or received by a station on the left section of the bus.

Table II

station	address
6	1011001
8	1011010

This means that a station on the section left of the address remapper - say station 5 - will address the other stations on the same section (or receive messages from these other stations) using their respective physical addresses - 1010010 and 1010011 for stations 7 and 9; on the other hand, it will address stations on the other section using their dummy address - 1011001 and 1011010 for stations 6 and 8.

Similarly, Table III gives the addresses of the stations on the left section of the bus, as they are sent and received by a station on the right section of the bus.

Table III

station	address
5	1011001
7	1011010
9	1011011

This means that a station on the section 4 right of the address remapper - say station 6 - will address the other station 8 on the same section (or receive messages from this other station) using its physical addresses 1010010; on the other hand, it will address stations 5, 7 and 9 on the other section using their dummy address - 1011001, 1011010 and 1011011.

When a message is sent from the station 6 on the right section 4 to the station 5 on the left section 3, the message is sent with an

address 1011001, that corresponds to the dummy address of station 5 for station 6. When the message is passed from the right section 4 to the left section 3, the address remapper changes the address into 1010001, so that the message on the left section is actually received by station 5. Similarly, when a message is sent from the station 7 on the left section 3 to the station 8 on the right section 4, the message is sent with an address 1011010, that corresponds to the dummy address of station 8 for station 7. When the message is passed from the left section 3 to the right section 4, the address remapper changes the address into 1010010, so that the message on the right section is actually received by station 8. In each case, the bits other than the address bits are left unchanged by the address remapper, so that the message is passed normally. Thus, the operation of the invention is transparent for each station, and the only constraint is the use of a different mapping of the stations on each section; this is easily obtained when programming each station. The invention thus permits using, on the same I2C bus, stations having the same address, or a number of stations larger than the configurable addresses of a given type of eeprom.

The operation of the invention was explained in reference to figure 1 in the case of one single remapper; in addition, the remapping of the addresses in figure 1 was simply done by changing one address bit. The invention is not limited to one address remapper, nor is it limited to this type of address remapping. More generally, a bus according to the invention may comprise more than one address remapper: each address remapper actually defines two sections - that is, one existing bus or bus section may be divided into two sections by an address remapper. The bus may thus comprise two remappers and three section, or n remappers and n+1 sections. The number of address remappers may be chosen according to the number of stations and to the address format: For instance, where stations with identical addresses are to be used on the bus, the number of sections would be at least equal to the number of such stations, each section containing one of the stations having identical addresses. Otherwise, where the address has a fixed part and a

configurable part, the number of sections may be chosen so that each section contains at most as many stations as the number of configurable addresses.

The address remapping scheme may simply be carried out as explained above, by changing the bits of the fixed part of the address; this solution is the simplest one to carry out where the address format of the stations comprises a fixed part. However, other remapping schemes are possible, even where the address format of the stations does not comprise a fixed part. It is in both cases sufficient that the dummy addresses for the stations out of a given section are different from the physical addresses of the stations in that given section. Changing at least one bit is a simple solution that fulfils this criterion.

Table IV gives the example of a bus system comprised of three sections, that is two address remappers; each section comprises three stations, having the physical addresses 1010001 and 1010010. The three sections are noted A1, A2 and A3, whereas the nine stations are noted S1 to S9. The columns of table IV give a possible remapping for each station.

Table IV

Station	Section A1	Section A2	Section A3
S1	1010001	1011001	1001001
S2	1010010	1011010	1001010
S3	1010011	1011011	1001011
S4	1011001	1010001	1000001
S5	1011010	1010010	1000010
S6	1011011	1010011	1000011
S7	1001001	1000001	1010001
S8	1001010	1000010	1010010
S9	1001011	1000011	1010011

In this example, the address remapper between sections A1 and A2 changes the value of the fourth bit of any address it receives. The address remapper between sections A2 and A3 changes the value of the third bit of any address it receives. The invention thus makes it

possible to have on the same bus nine stations, that is more than the number of possible addresses using an address format of the type 1010xyzR. It also make it possible to have on the same bus several stations having the same physical address, e. g. S1, S4 and S7 in Table IV.

Figure 2 is a schematic diagram of an address remapper according to the invention; the address remapper of the invention is preferably able to change the address it receives on one section into addresses remapped for another section. Preferably, the remapper of figure 2 is able to change or remap the address in a manner transparent to the station, that is without inducing any significant delay in the transmission of messages. Such a real time transmission ensures that the different sections of the bus will remain synchronised, so that the operation of the invention is transparent for the stations. In addition, this ensures that the time out period, in case there is one, does not lapse: under I2C existing specifications, there is no time out, however, there is a time out of 25 ms in the SMBus specifications. This also allows several remappers to be cascaded along the bus.

The address remapper of figure 2 is designed for transfer of master to slave messages in one direction only, in the example of figure 2, from the left to the right; responses from slaves may be transferred in the other direction. In other words, the remapper of figure 2 is designed to be used with all stations that can possibly act as masters on the left side of the remapper. Such a configuration may prove useful for instance where the I2C bus is used for hardware management purposes, and where some stations need only be addressed as slave stations; thus, they may be wired on a bus section containing only slave stations, while the other bus section will contain stations acting as slave or master.

The remapper comprises left data and clock terminals 21 and 23, and right data and clock terminals 22 and 24; respective sections of the bus may be connected to the left and right terminals. The left and right clock terminals 23 and 24 are connected, so that the clock

wire along the different bus sections is continuous; this ensures synchronism of the different bus sections. The left and right data terminals 21 and 22 are connected via switching means 26; the switching means are able to connect or disconnect the left and right data terminals, and mainly comprise a switch 27 and a switch command 28. The remapper of figure 2 further comprises START detecting means 30 connected between the left data and clock terminals 21 and 23, for detecting the occurrence of a START condition on the section of the bus connected to the left data and clock terminals. The START detecting means 30 output a signal representative of the occurrence of a START condition to control means 32. The remapper of figure 2 further comprises bit setting means 34 connected to the right data terminal 22, for setting the value of a bit on a data wire connected to the right data terminal. The control means 32 control the operation of the switching means 26 and of the setting means 34 as explained below; the control means are also connected to the clock line. The control means, the switching means and the bit setting means form address remapping means for remapping the address received on the left terminals and transmitting the remapped address to the right terminals.

The different elements of the remapper of figure 2 may easily be realised by the person skilled in the art, with the same type of components used for I2C stations; inter alia, the START detecting means and the bit setting means are usual components of any station for I2C buses; for instance, the bit setting means may be formed of pull-down means for setting the value of a bit to 0, the pull-down being inactivated when the bit value is 1.

Figure 3 shows the timing of signals in a two wire serial bus; change of data on the data wire SDA is allowed in the low period t_{low} of the clock wire SCL. $t_{HD;DAT}$ is the data hold time between the falling edge of a clock pulse and the beginning of the change of data on the data wire; this period is specified under I2C and may be zero; $t_{SU;DAT}$ is the data set-up time between the setting up of the data on the data wire and the leading edge of the following clock

pulse. A START condition is detected when the data signal goes down during the high period t_{high} of the clock signal.

Figure 4 is a flowchart of the operation of the address remapper of figure 2; the operation is described in reference to the example of figure 2, whereby the address remapper changes the value of the fourth bit of each address it receives.

At step 40, the control means 32 check whether a START condition was detected, that is whether the START detecting means output a signal representative of the detection of a START condition. At that time, the switching means are closed, so that the data wires connected to the left and right data terminals are connected. Thus, the START condition may be output by any station on any section of the bus. If no START condition is detected, the process stays at step 40. If a START condition is detected, the process passes to step 42.

At step 42, the control unit sets a delay of three clock periods. At the end of these three clock periods, the process passes to step 44. This delay corresponds to the operation of the remapper, where the first three bits of the address are not changed. While the process is at step 42, the switch means remain closed, so that the first three bits of the address are not changed by the remapper.

At step 44, the falling edge of the clock signal is detected; at that time, the third address bit has just passed; if this is necessary, a delay of $t_{HD;DAT}$ is set. The process then passes to step 46.

At step 46, the value of the fourth bit of the address is changed. For this, the switching means are opened, so that the data wire on the two section of the bus connected to each side of the remapper are isolated; at the same time, the control means 32 output a control signal to the bit setting means, that is opposite to the signal received on the left data terminal. Thus, the bit value on the right data terminal is set to the value opposite the bit value on the left data terminal, with a delay corresponding to the

propagation time through the control means; the value of such a delay is far less than the data set-up time, so that the setting of the value on the right data terminal occurs in due time. The process then passes to step 48.

At step 48, the falling edge of the clock signal is detected; if necessary, a delay of $t_{HD;DAT}$ is set, and the switch means are then closed, while the bit setting means are inactivated. The process then passes again to step 40.

The flowchart of figure 4 may be adapted to change more than one bit, or to change another bit than the fourth one. The operation is in any case similar, the switch means being opened and the bit setting means being activated whenever a bit need to be changed.

Figure 5 is a schematic drawing of an address remapper according to the invention, that may be used for bidirectional transfer. The remapper of figure 5 is similar to the one of figure 2; it however further comprises left bit setting means 51 connected to the left data terminal 21, for setting the value of a bit on a data wire connected to the left data terminal; it also comprises right start detecting means 52 connected to the right data and clock terminals for detecting a START condition on the section of the bus connected to the right terminals. In addition, the control means receive the signal from the right data terminal. Thus, the address remapper comprises:
right and left bit setting means 34 and 51;
right and left start detecting means 52 and 30.

The operation of the remapper of figure 5 is the following. When a START condition is detected on one section of the bus, the remapper remaps the address received from this section of the bus. For instance, if a START condition is received on the section of the bus connected to the right terminals, the right bit setting means are inactivated, and the address received from the right side is remapped to the left side by the left bit setting means, in a way similar to the operation of the remapper of figure 2.

Thus, the remapper of figure 5 allows remapping on sections of the bus on both sides of the remapper; it may be used where there are masters on both sides of the remapper.

The operation of the remapper of figure 2 is based on the fact that any address sent on the bus immediately follows a START condition; in case of a different protocol, the START detecting means could be changed so as to detect the fact that an address is going to be sent on the bus: the START detecting means of figures 2 and 4 thus actually constitute address detecting means for the I2C bus. More generally, the operation of the remapper may be adapted to the communication protocol used on the bus; for instance, it is not necessary that the START detecting means try to detect a START when there cannot be one, e.g. during data transfer: under such circumstances, the START detecting means could be inactivated, and could be reactivated only when a START is possible.

It should be understood that the invention is not limited to the example of a serial bus discussed above. The invention also applies to different types of serial buses, and also to parallel buses. In the case of a parallel bus, remapping one bit of an address simply involves changing the level on one wire of the parallel bus, when the address is actually being applied on the bus. The address detecting means are thus preferably adapted for detecting the conditions under which the address is applied on the bus.

In addition, the invention is not limited to the binary values used in the I2C bus. In other words, the address remapping means could bring one wire or more to the high level. A start condition could be associated with a transition on one wire while the other one is at a low level.

[CLAIMS]

1. A bus, having at least an address remapper (1) defining two sections (3, 4) in the bus, each section comprising at least one station (5-9) having a physical address, wherein a station on one section of the bus is assigned a dummy address for being addressed by a station on the other section, the address remapper remapping a dummy address from the other section into a physical address to the one section.

2. A bus according to claim 1, wherein the format of a physical address comprises a fixed part and a setable part, and wherein the dummy address is obtained by changing at least one bit of the fixed part of the physical address.

3. A bus according to claim 1 or 2, wherein the dummy addresses for stations out of a given section are different from the physical addresses for stations in said given section.

4. An address remapper for a bus, comprising
- terminals (21-24) for connecting two sections of the bus;
- address detecting means (30) for detecting an address received from one section of the bus;
- address remapping means (32, 26, 34) for remapping the address and transmitting the remapped address to the other section of the bus.

5. An address remapper according to claim 4, wherein the bus is a two wire serial bus, and wherein the address detecting means (30) detect a transition of the value on one wire while the other wire is a given level.

6. An address remapper according to claim 4 or 5, wherein the bus is a two wire serial bus, and wherein the address remapping means comprise means (34) for bringing one wire to a given level.

7. An address remapper according to claim 4, 5 or 6, wherein the bus is a two wire serial bus having one data wire and one clock wire,

the terminals (23, 24) for the clock wire of each section being connected.

8. An address remapper according to claim 7, wherein the address remapping means comprise switching means for selectively connecting the terminals (21, 22) for the data wire of each section.

10. A process for connecting two sections of a bus, by transmitting data from one section of the bus to the other section of the bus, comprising the steps of

- detecting an address sent from one section of the bus to the other section of the bus;
- remapping the address before transmitting it to the other section of the bus.

11. A process according to claim 10, wherein the step of detecting comprises detecting a START condition preceding an address.

12. A process according to claim 11, wherein the step of remapping comprises changing at least one bit of an address, preferably one bit of a fixed part of an address.

[ABSTRACT]

Address remapping for a bus

The invention relates to an address remapper (1) for a two wire serial bus. This remapper connects two sections (3, 4) of the bus, and is generally transparent, except when it receives an address; in this case, the remapper changes the address before transmitting it to the other section of the bus. This allows using stations having the same physical address on the same bus, and allows a greater number of stations to be used on the bus larger than that allowed under an address format with a fixed part.

(Fig. 1)

FIG_1

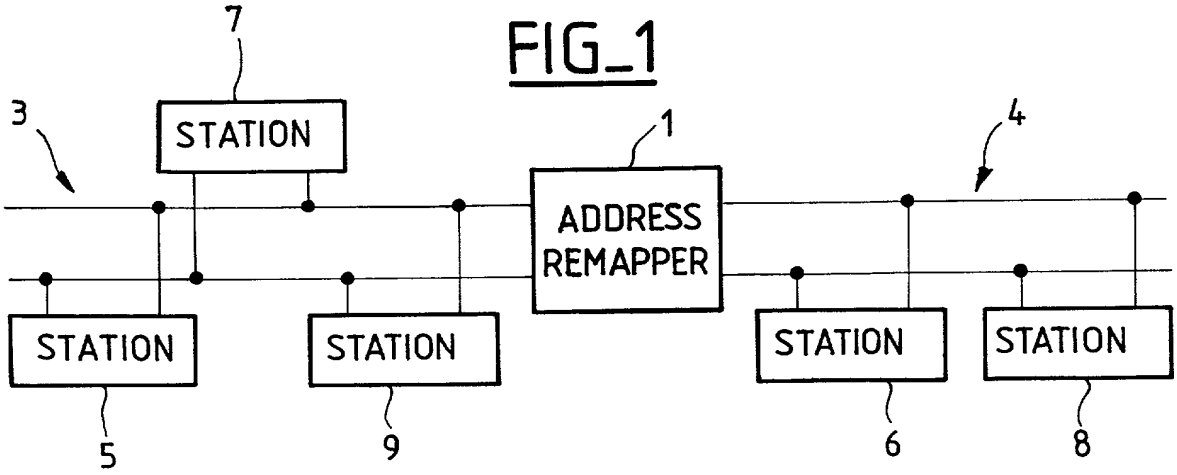


FIG_2

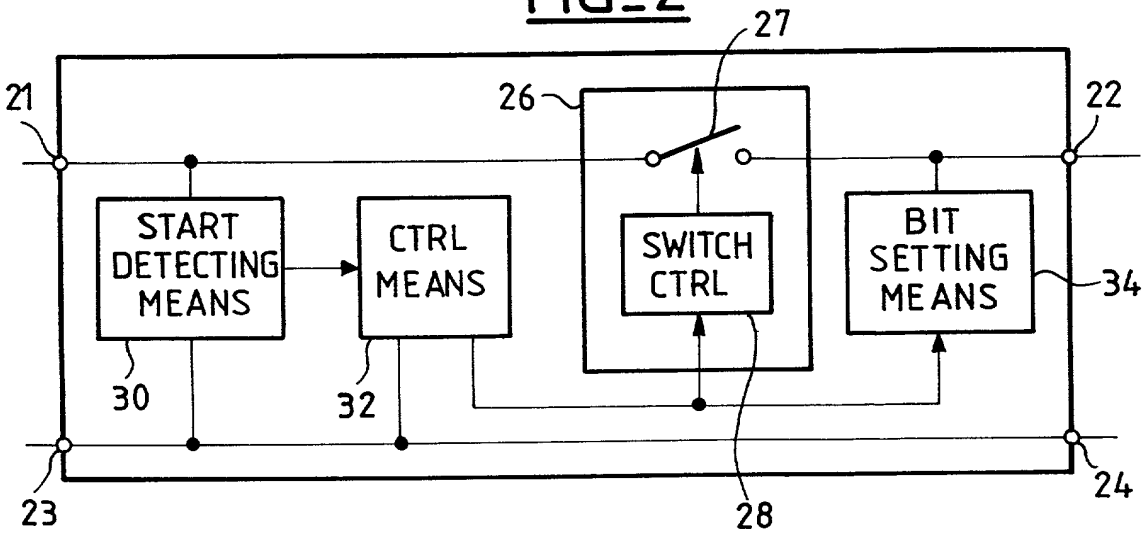
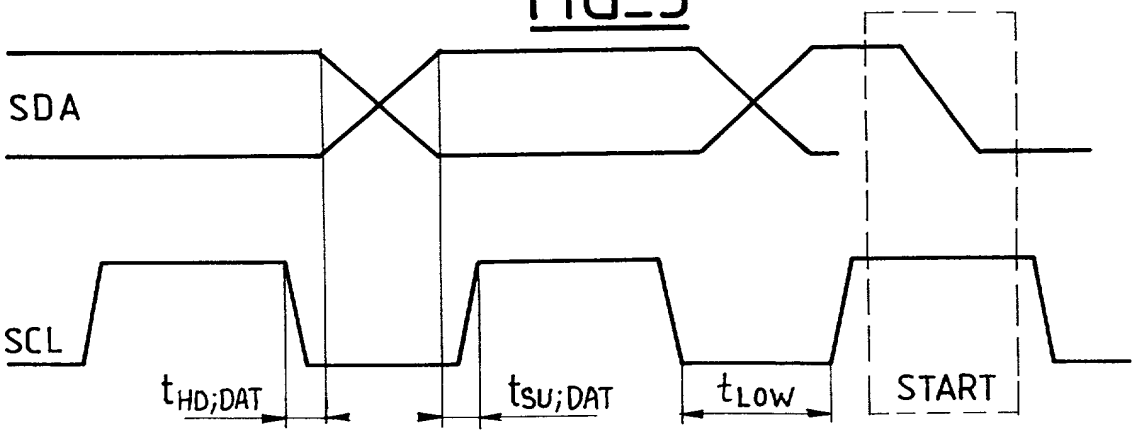


FIG_3



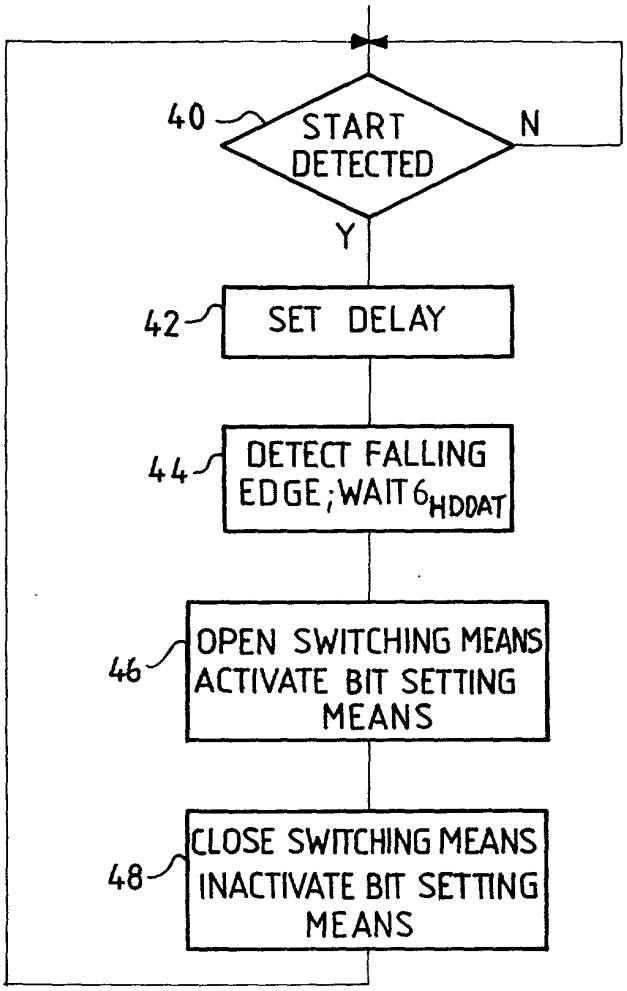
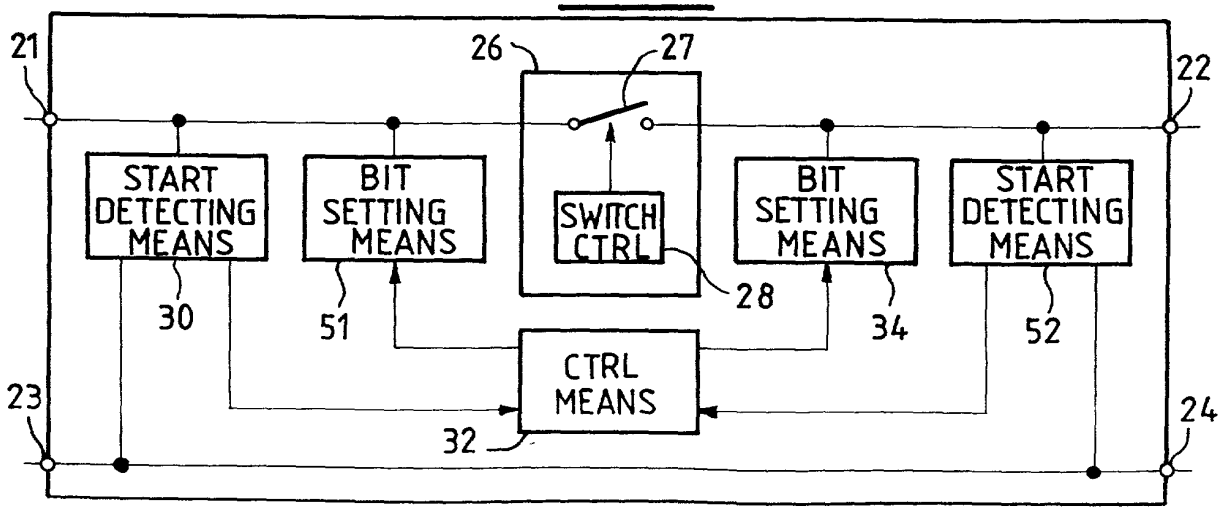

40
START DETECTED
N
Y
42
SET DELAY
44
DETECT FALLING EDGE; WAIT 6_{HDDAT}
46
OPEN SWITCHING MEANS
ACTIVATE BIT SETTING MEANS
48
CLOSE SWITCHING MEANS
INACTIVATE BIT SETTING MEANS

FIG_4

FIG_5


21
26
27
22
START DETECTING MEANS
BIT SETTING MEANS
SWITCH CTRL
BIT SETTING MEANS
START DETECTING MEANS
30
51
28
34
52
CTRL MEANS
23
32
24

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

Attorney's Docket No.: 50980001US

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

"Address Remapping for a Bus"

the specification of which

X is attached hereto;

_____ was filed on _____ as Application Serial No. _____, and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

Prior Foreign Application(s)				Priority Claimed	
98400760.9	Europe	27/03/98		X Yes	No
Number	Country	Day/Mo/Yr Filed			
				Yes	No
Number	Country	Day/Mo/Yr Filed			
				Yes	No
Number	Country	Day/Mo/Yr Filed			

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56, which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial #)	(Filing Date)	(Status) (patented, pending, abandoned)

POWER OF ATTORNEY: As a named Inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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